

6408382

SERIAL NO.: 09/422,015
PETER H. PRIEST (919-942-1434)

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FIG. 1A

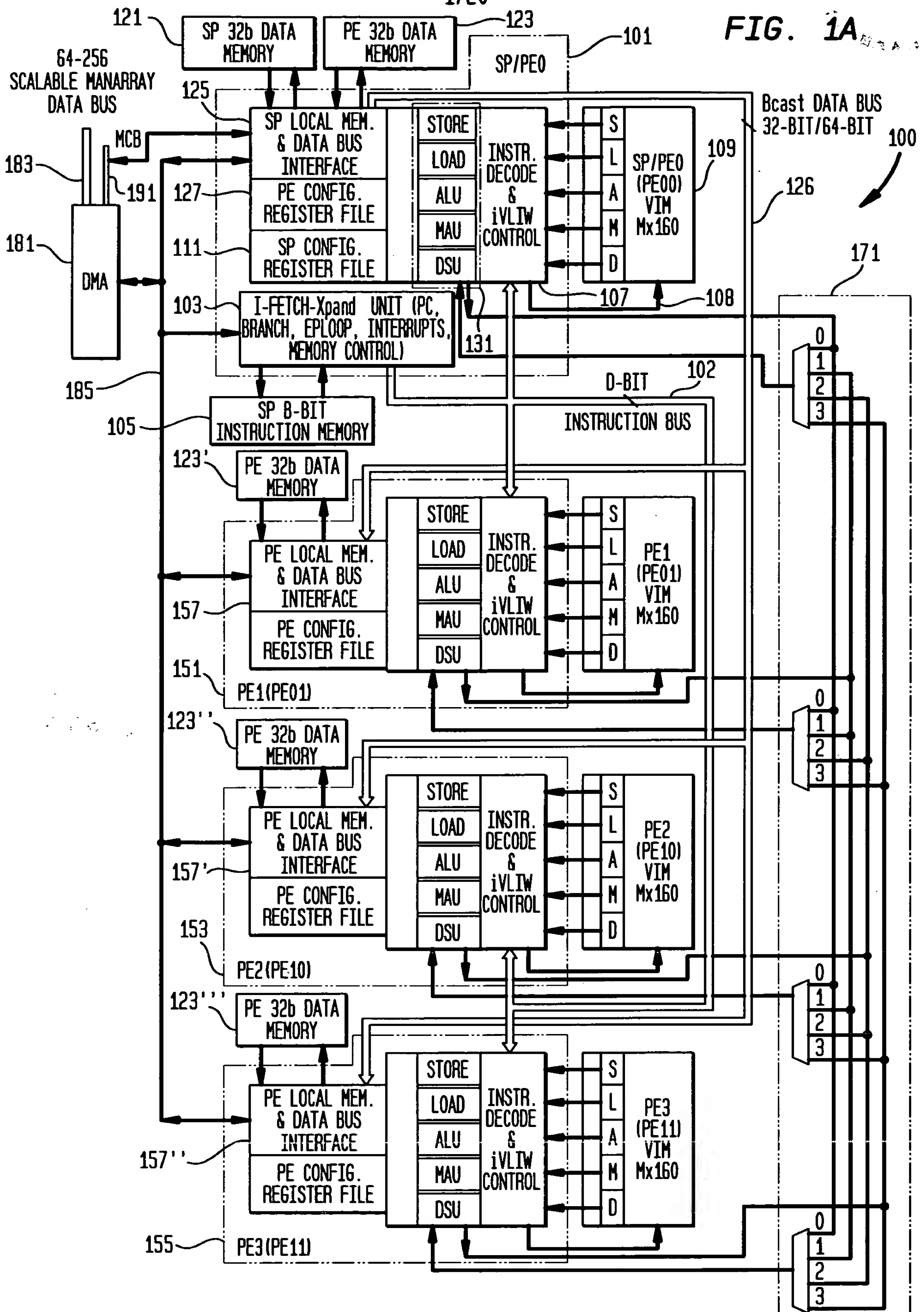
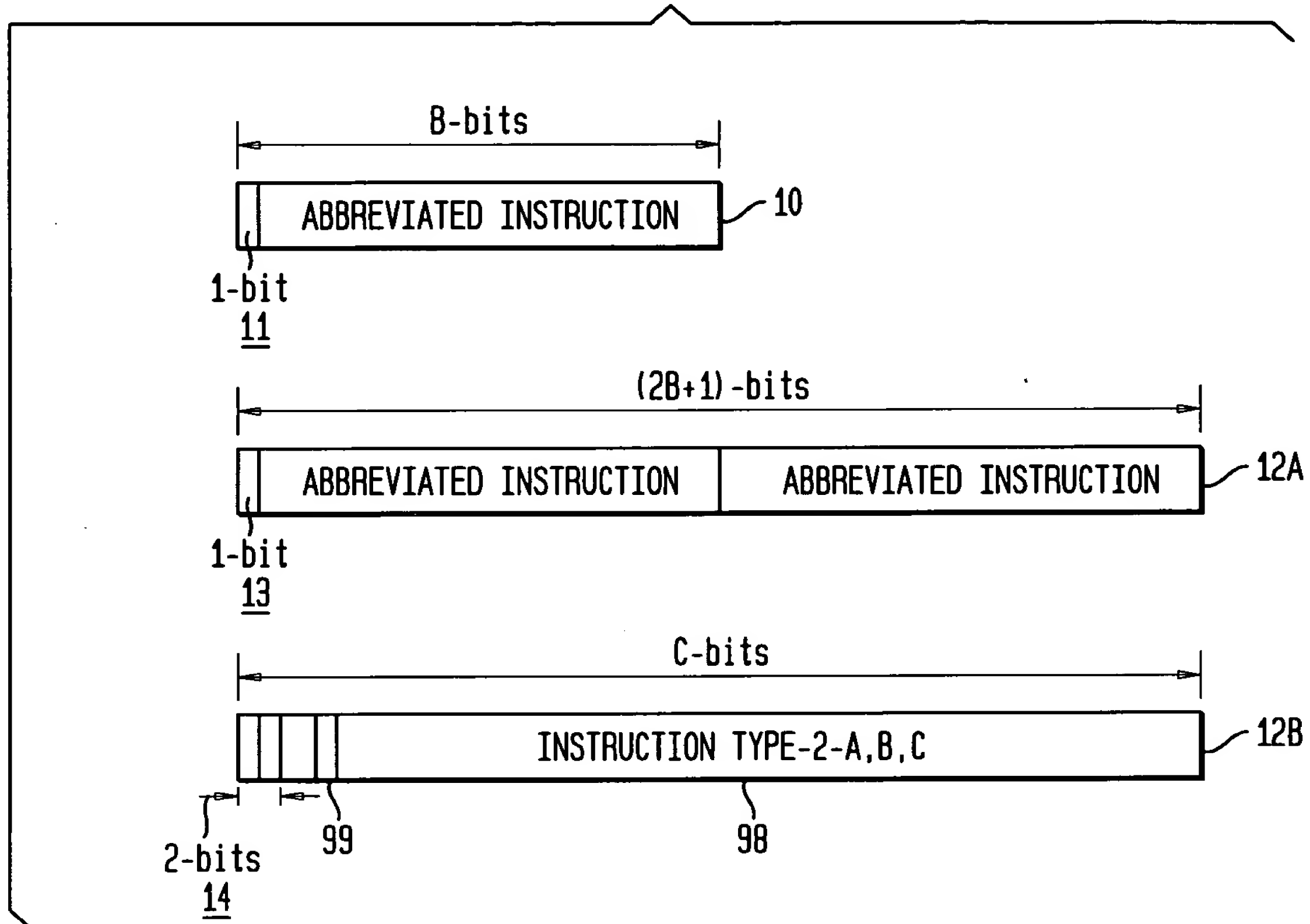




FIG. 1B



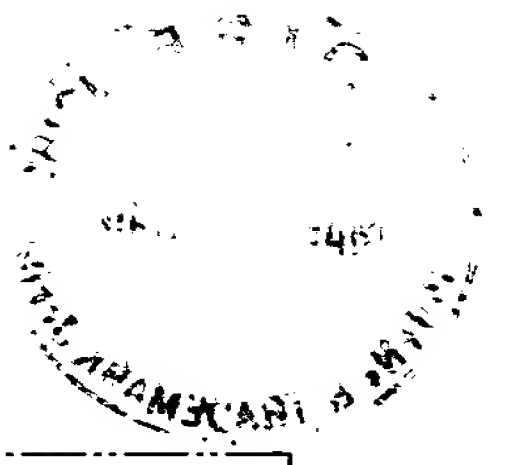
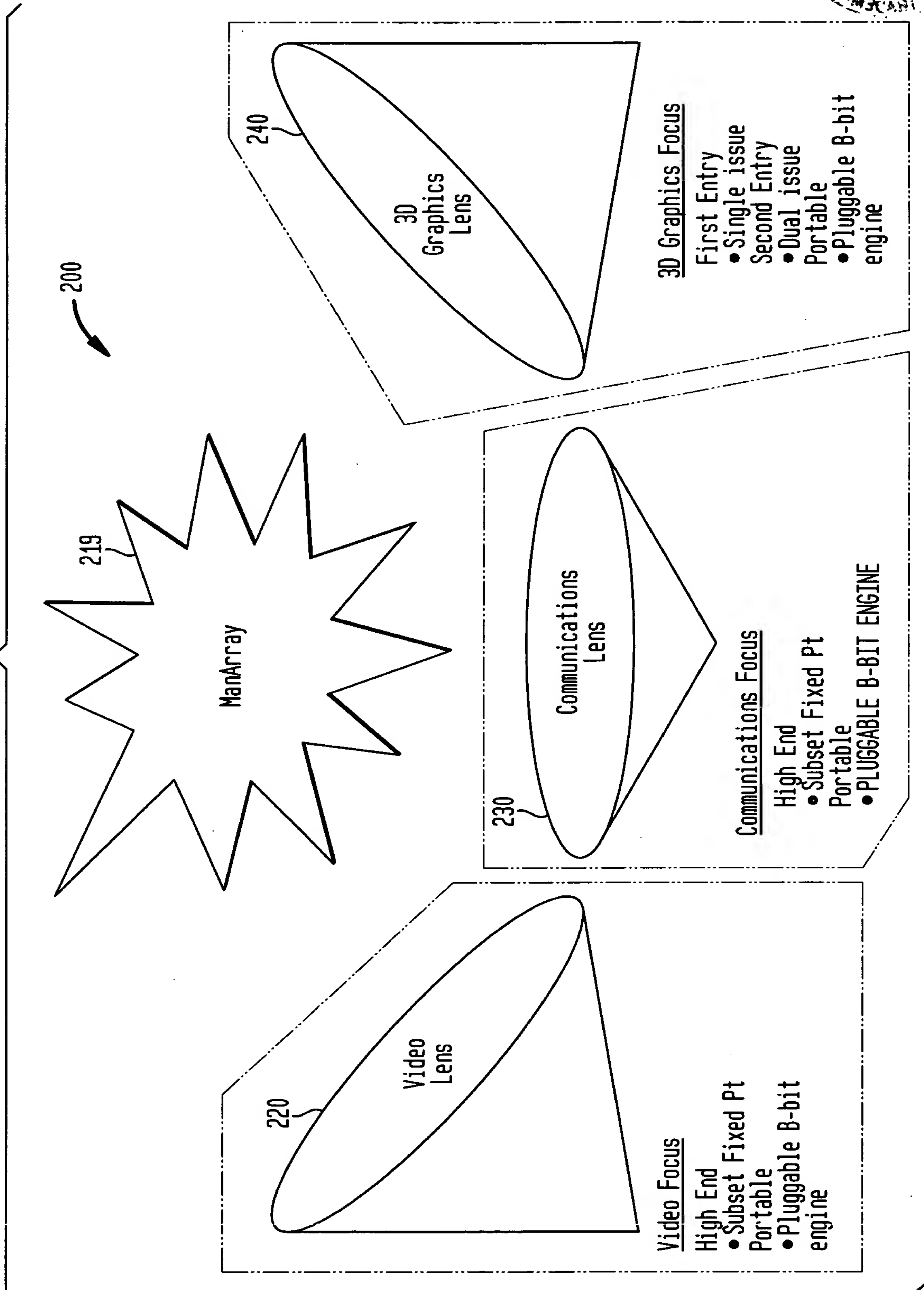


FIG. 2



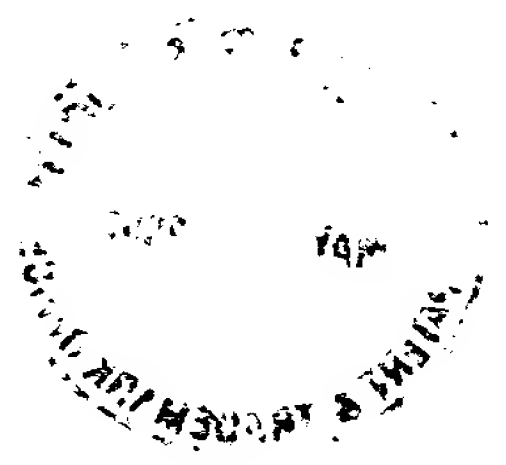
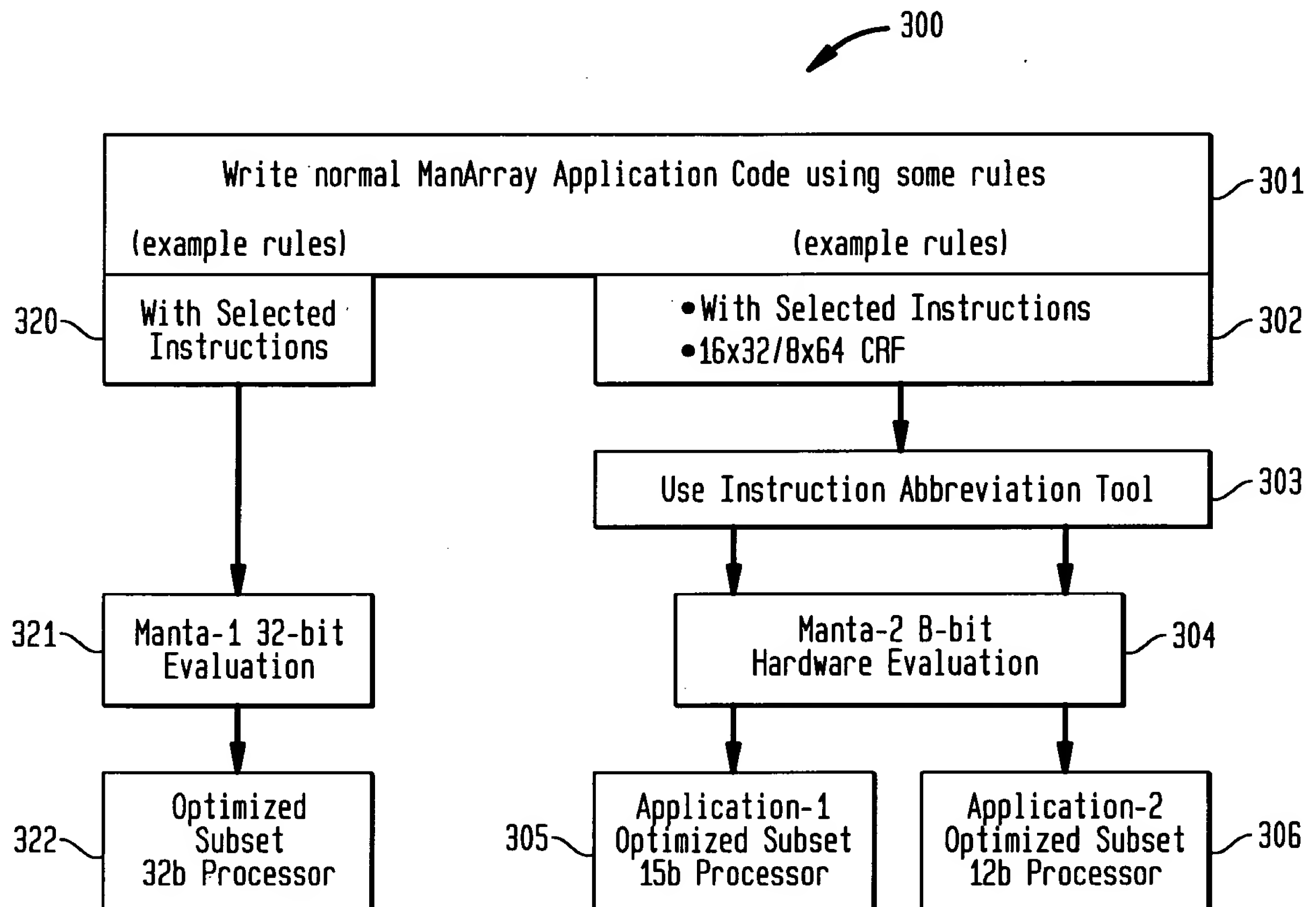


FIG. 3A



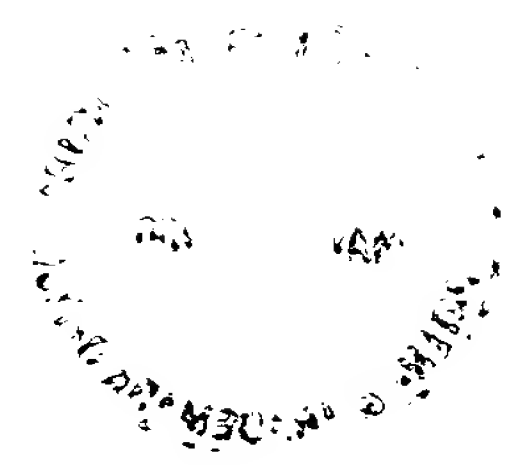


FIG. 3B

10

330				340											
B-1				0											
335															
	B-2	B-3	B-4	B-5											
S/P	1	0	0	Store											
	1	0	1	Load											
	1	1	0	ALU											
	1	1	1	MAU											
	1	0	0	DSU											
	1	0	1	Control Flow											
	1	1	0	Set V and LV iVLIW											
	1	1	1	XViVLIW											

341
342
343
344
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346
347
348

FIG. 3C

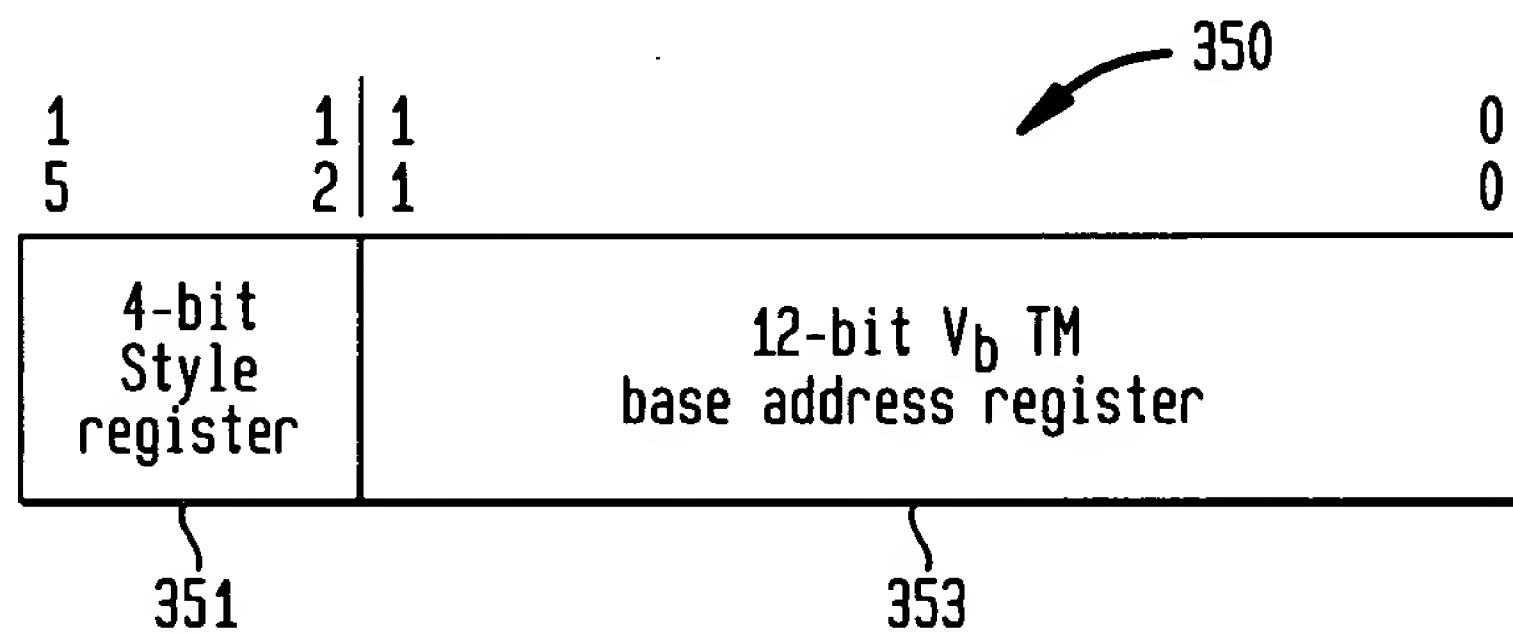


FIG. 3D

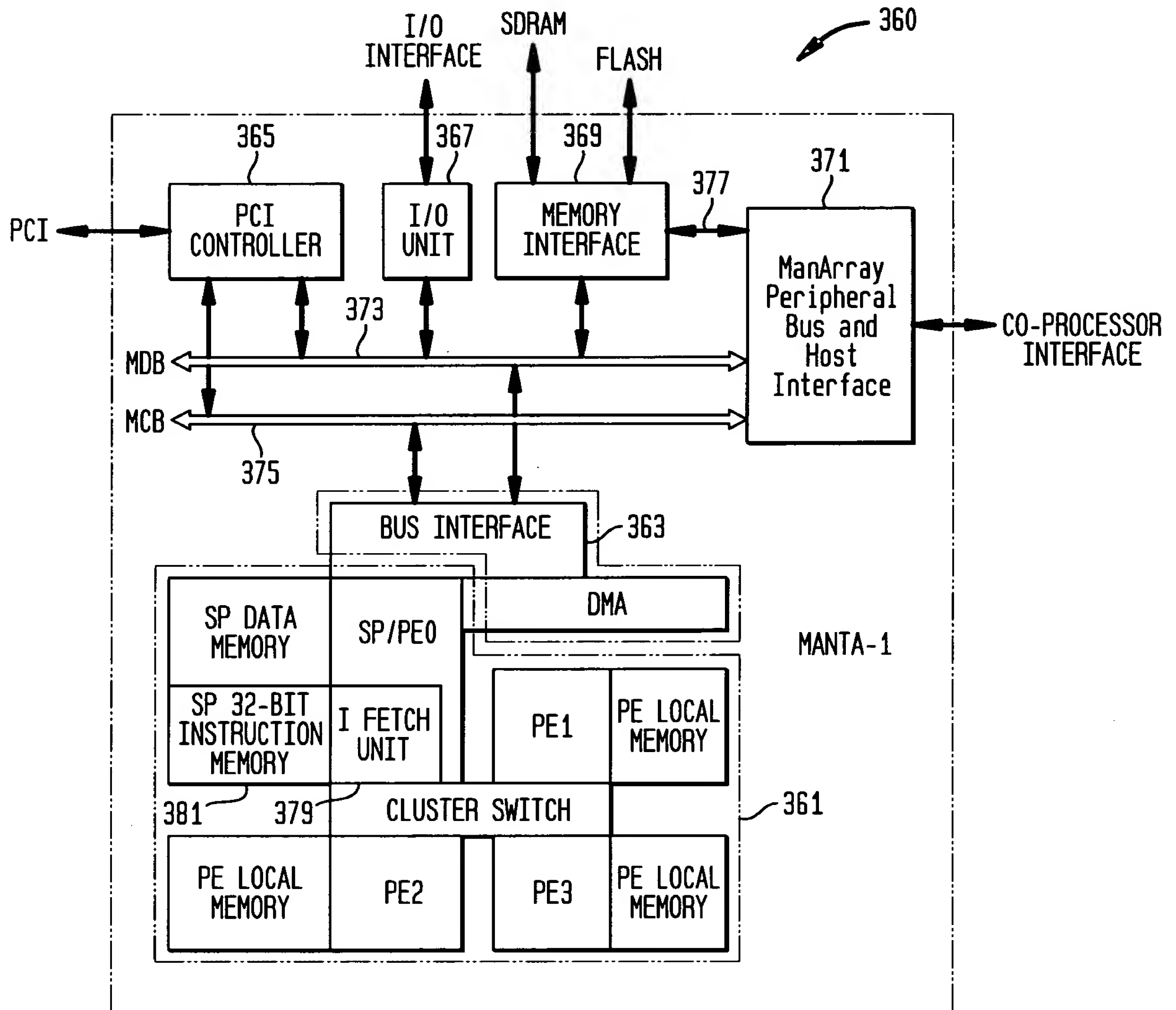
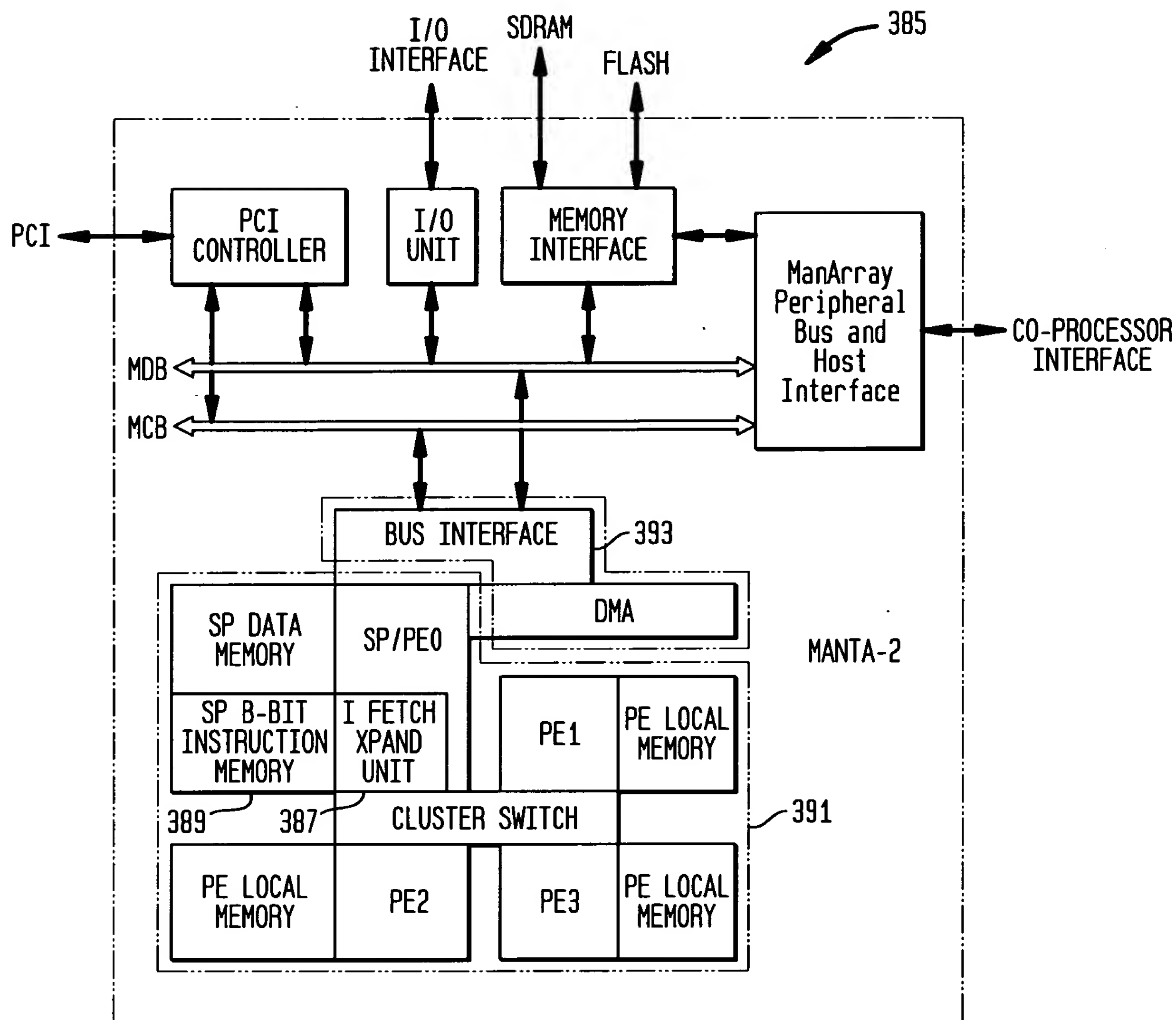
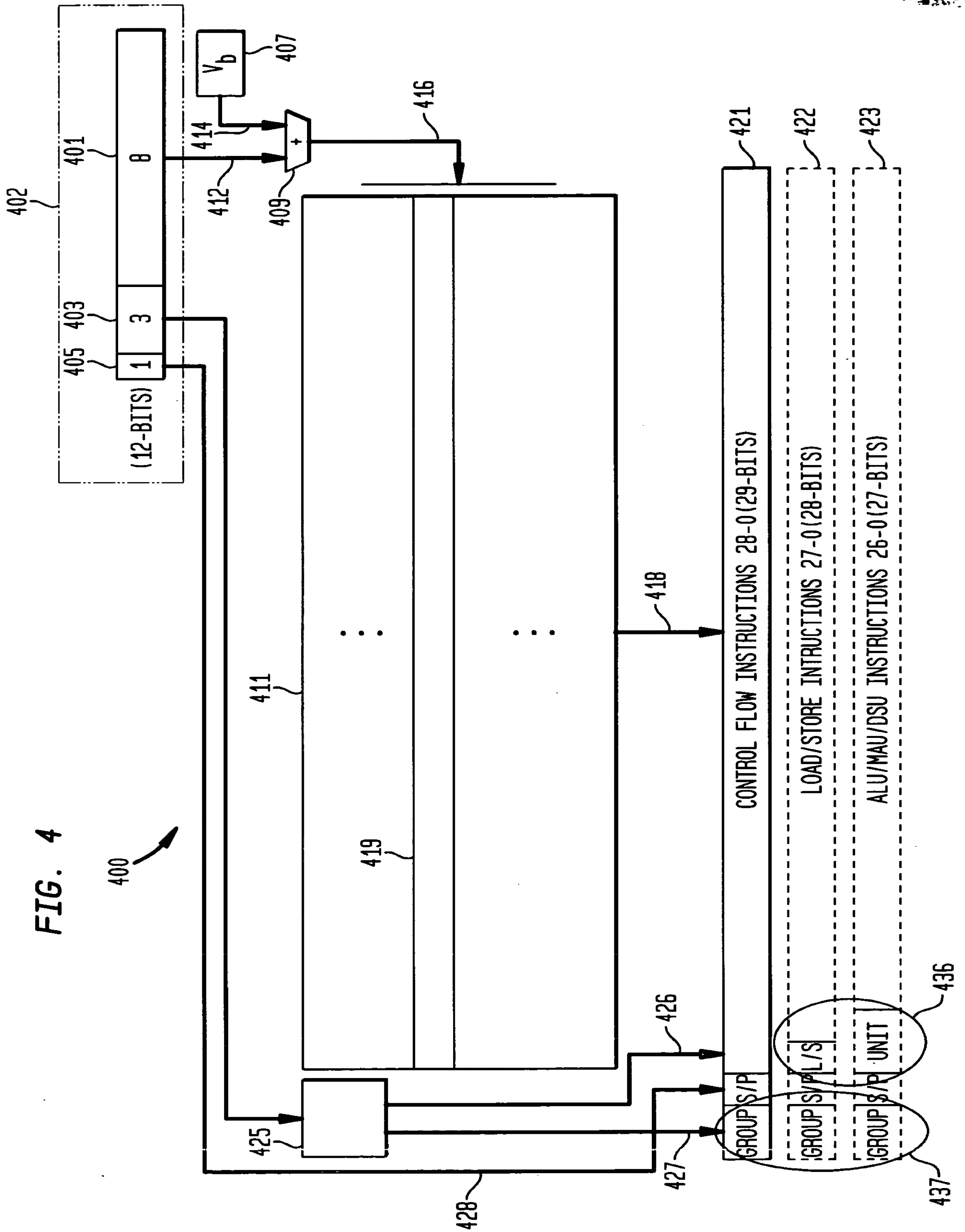


FIG. 3E





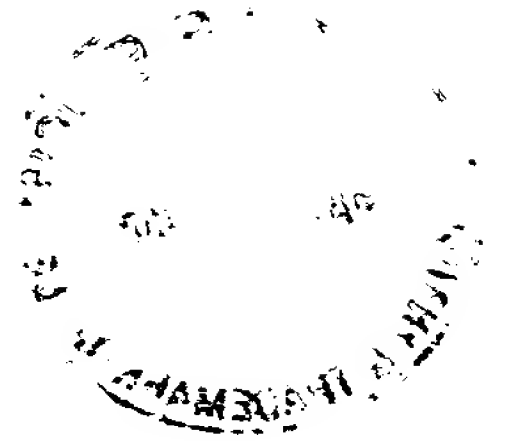
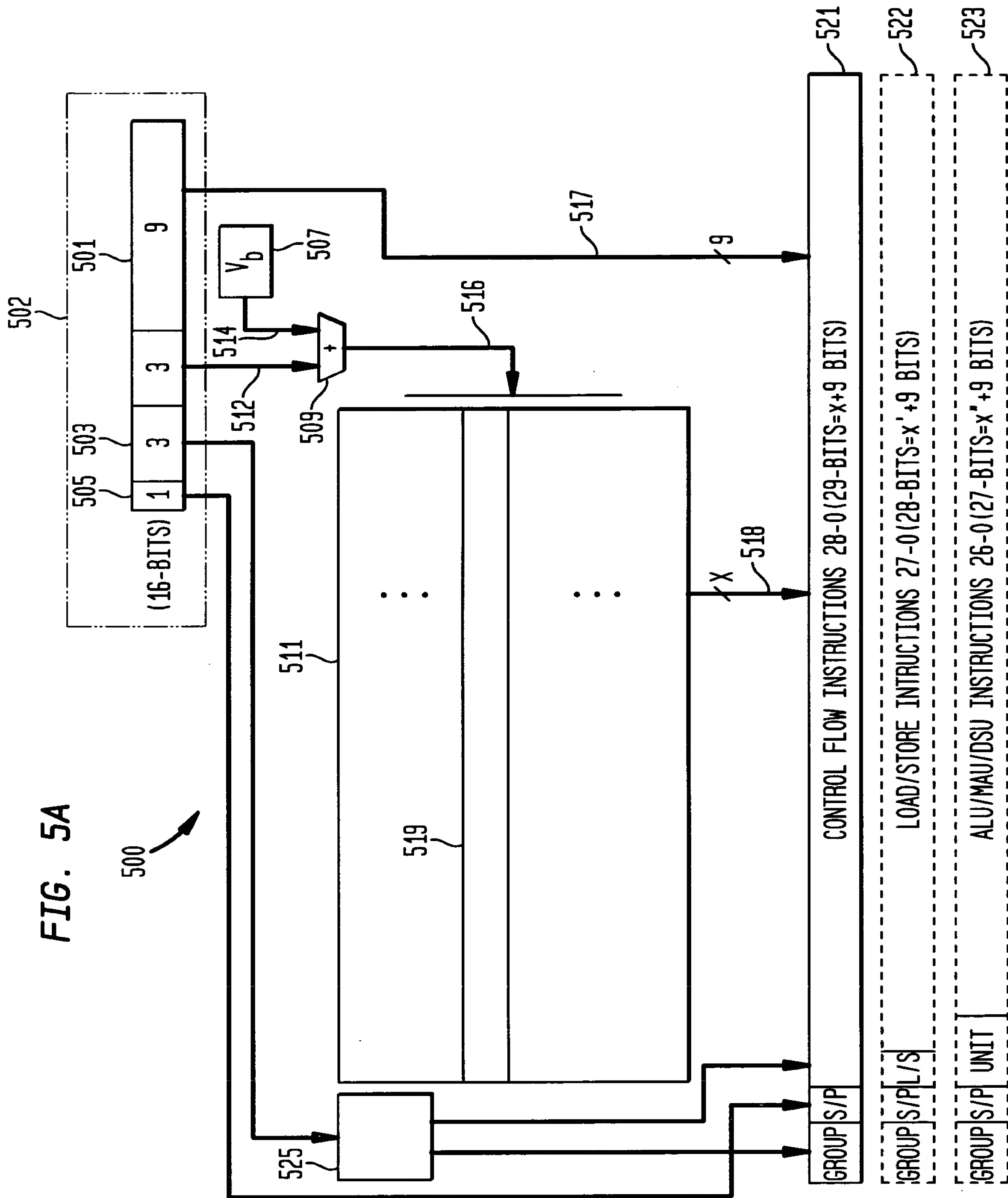


FIG. 5A



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FIG. 5B

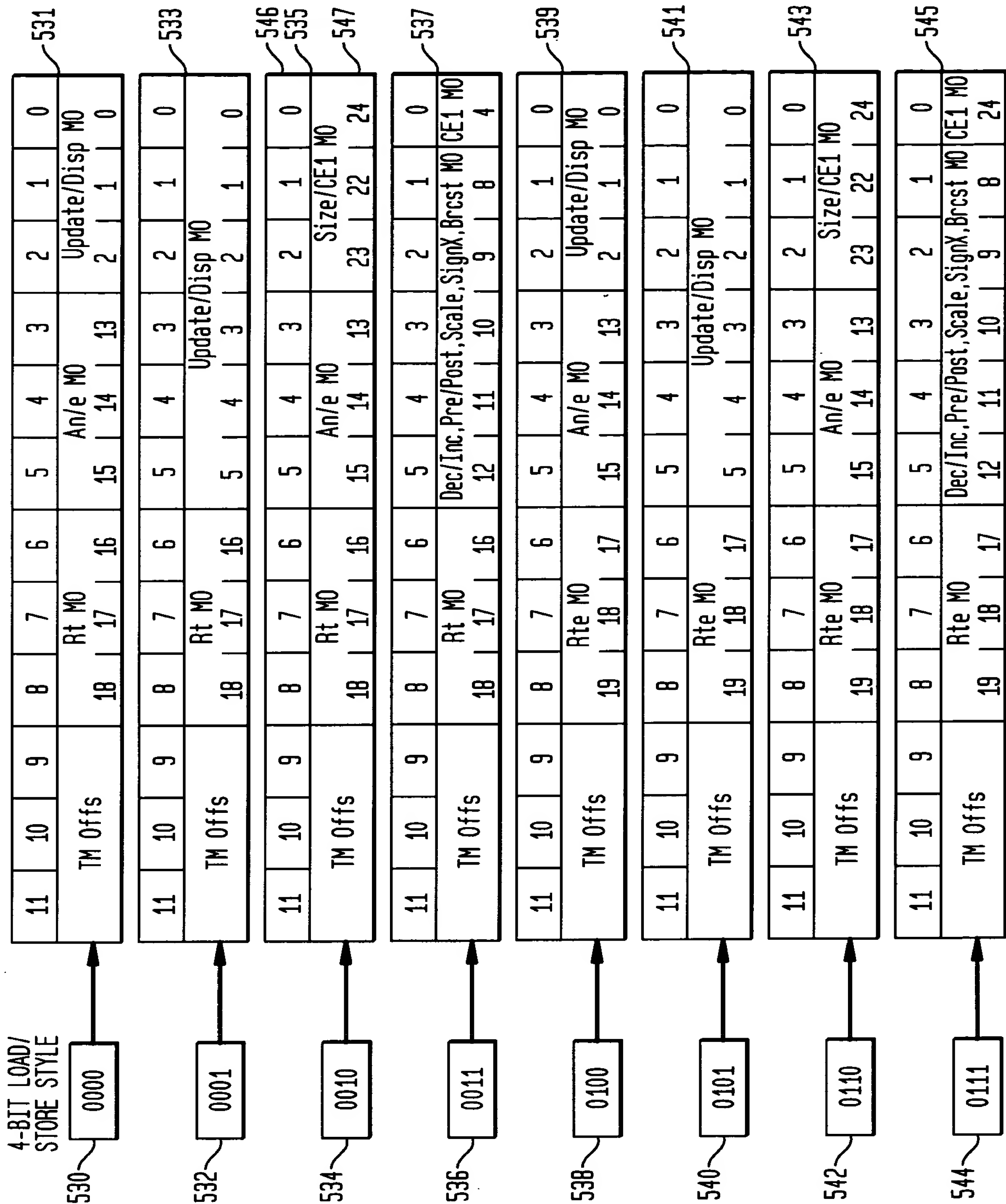
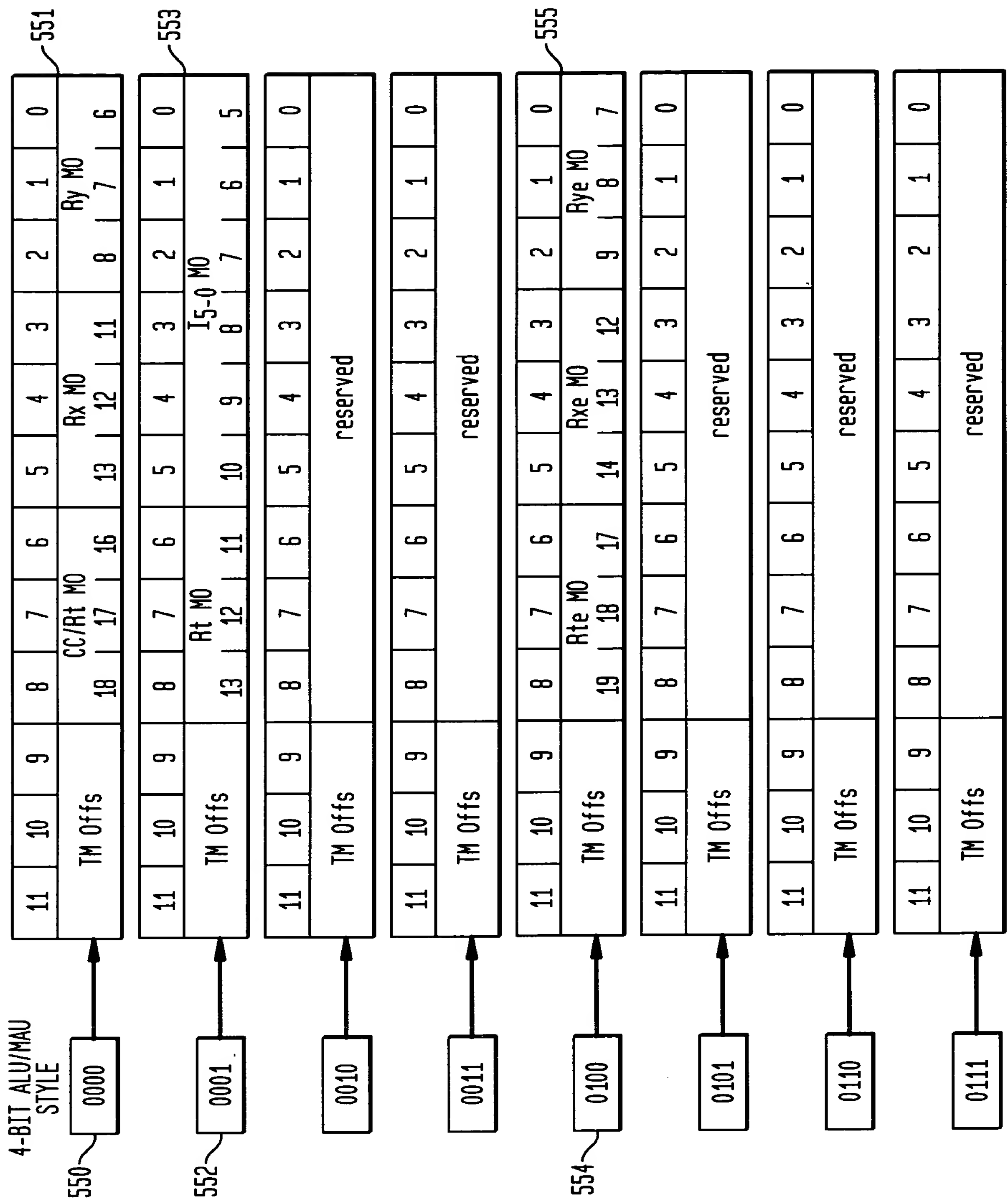


FIG. 5C



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FIG. 5D

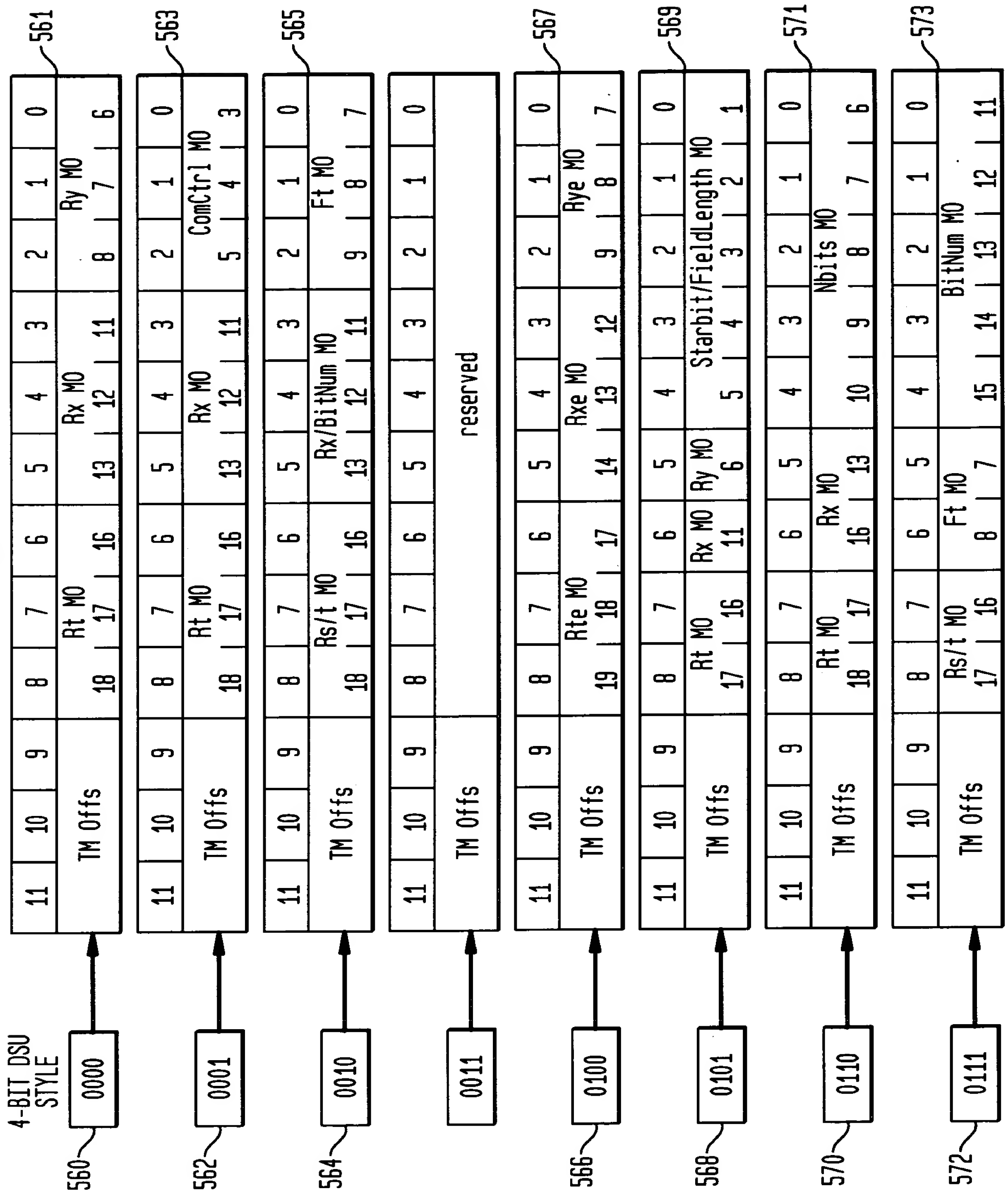




FIG. 5E

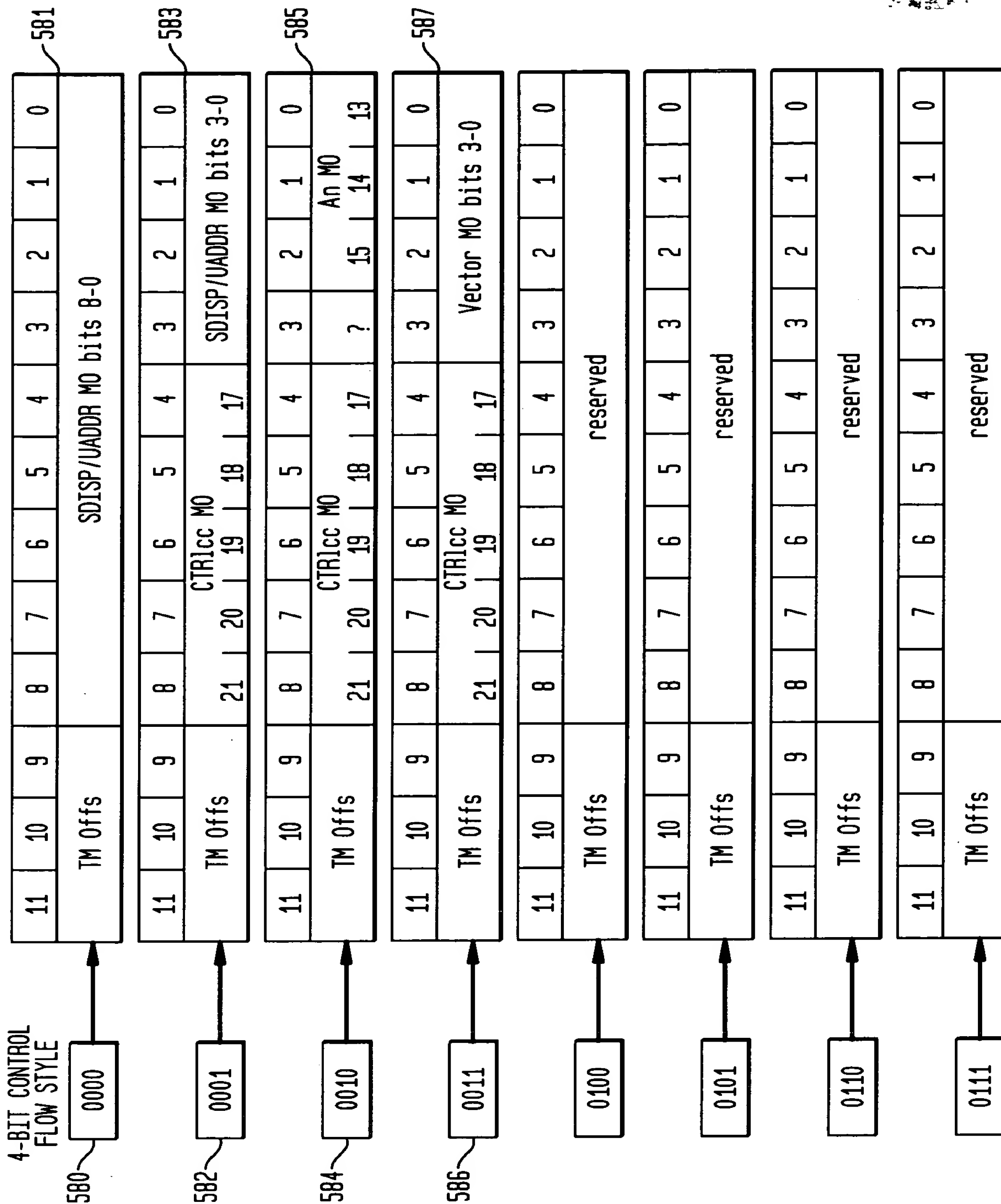


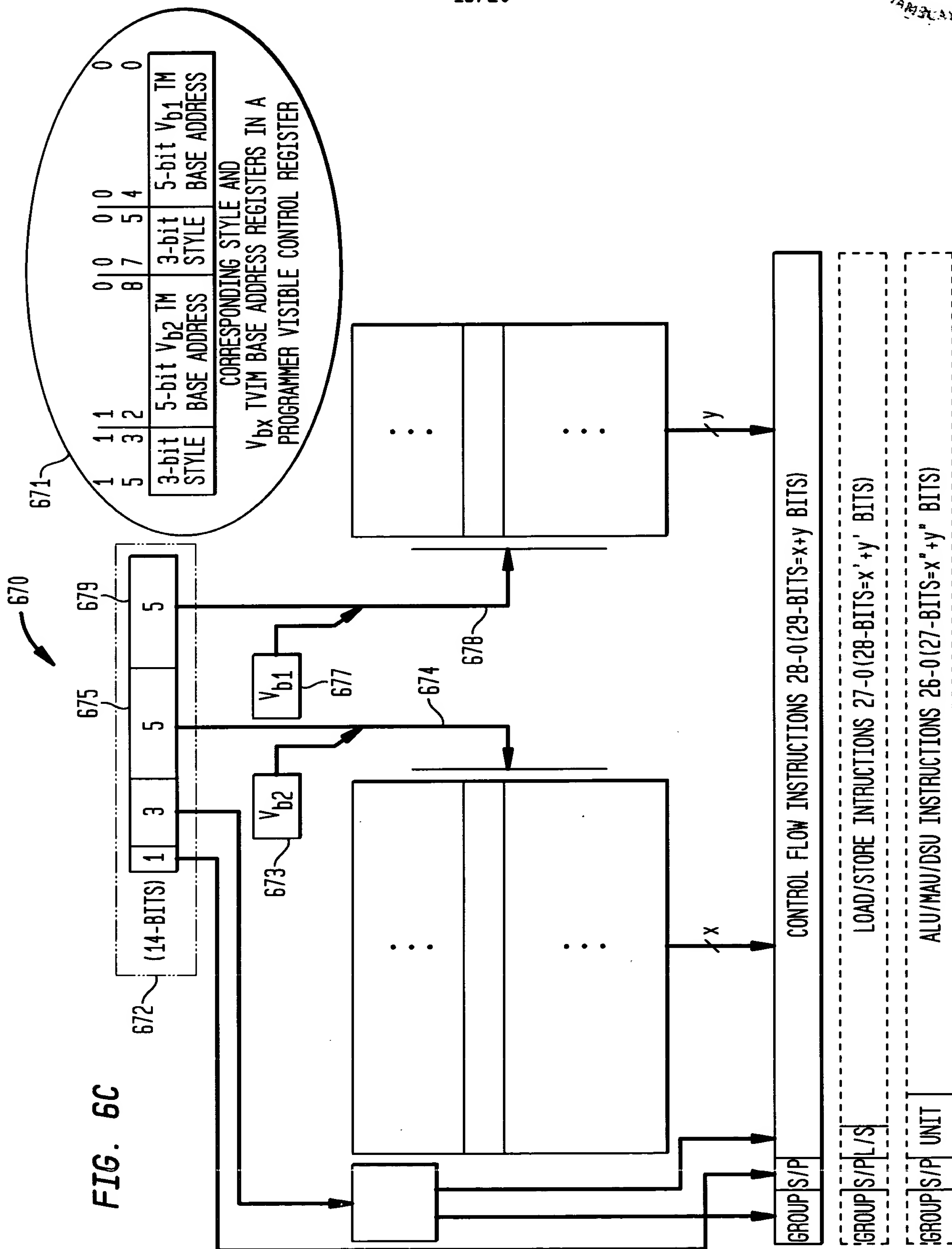


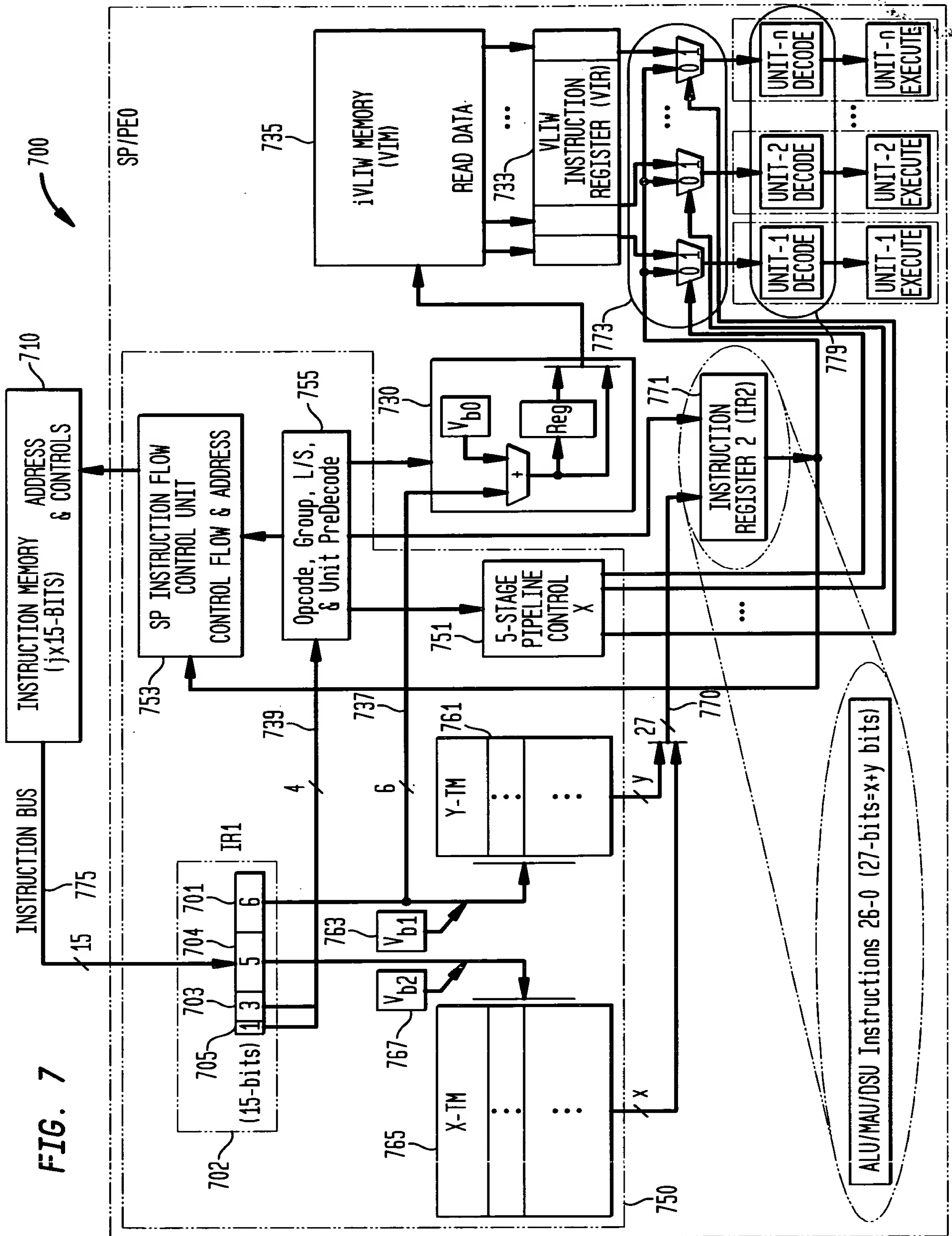
FIG. 6B

650

13	12	11	10	9	8	7	6	5	4	3	2	1	0								
S/P	XV iVLIW 111			4-BIT TM20ffs Vb=V0				6-BIT TM10ffs Vb=V0													
652														656				654			

670





800

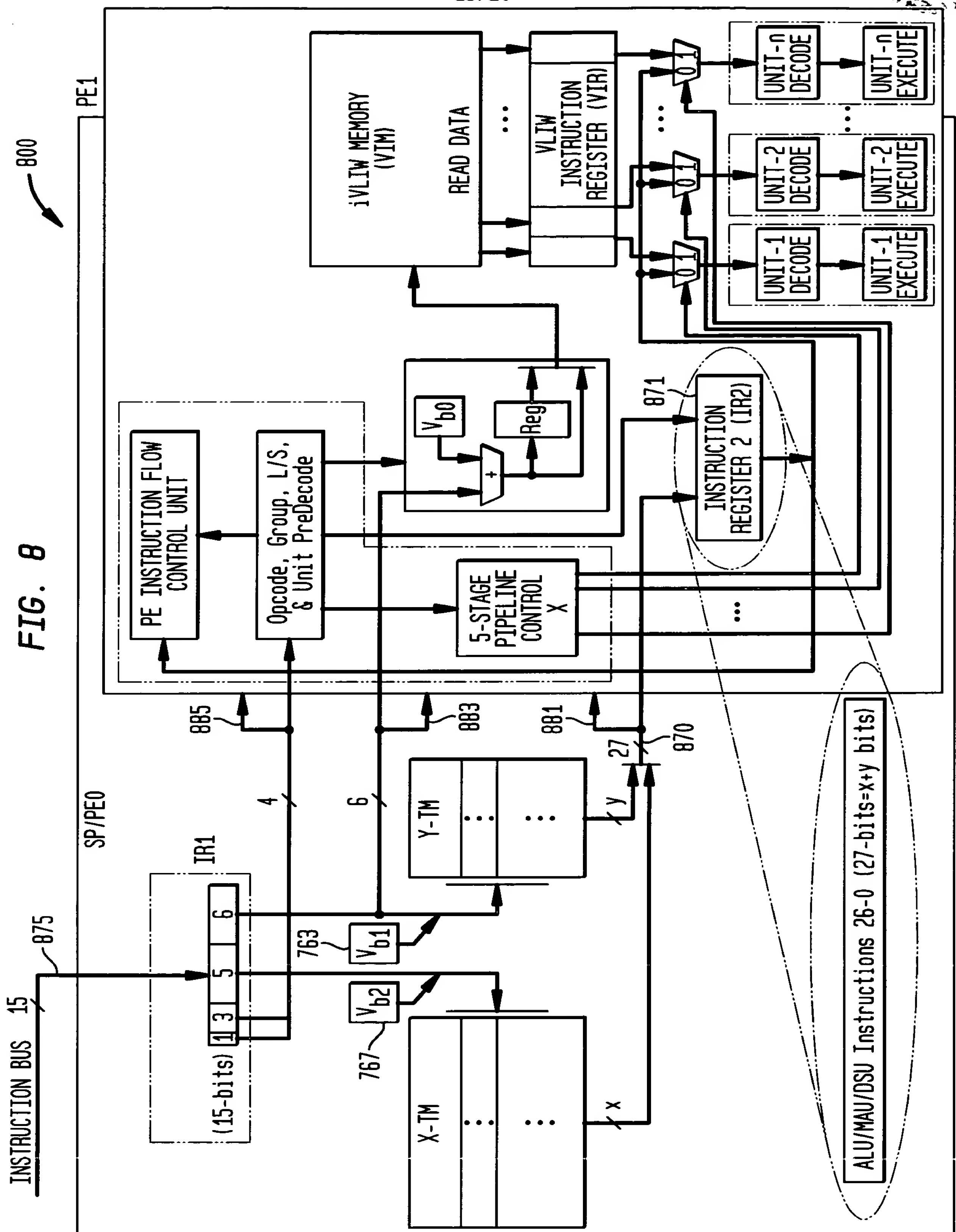


FIG. 9

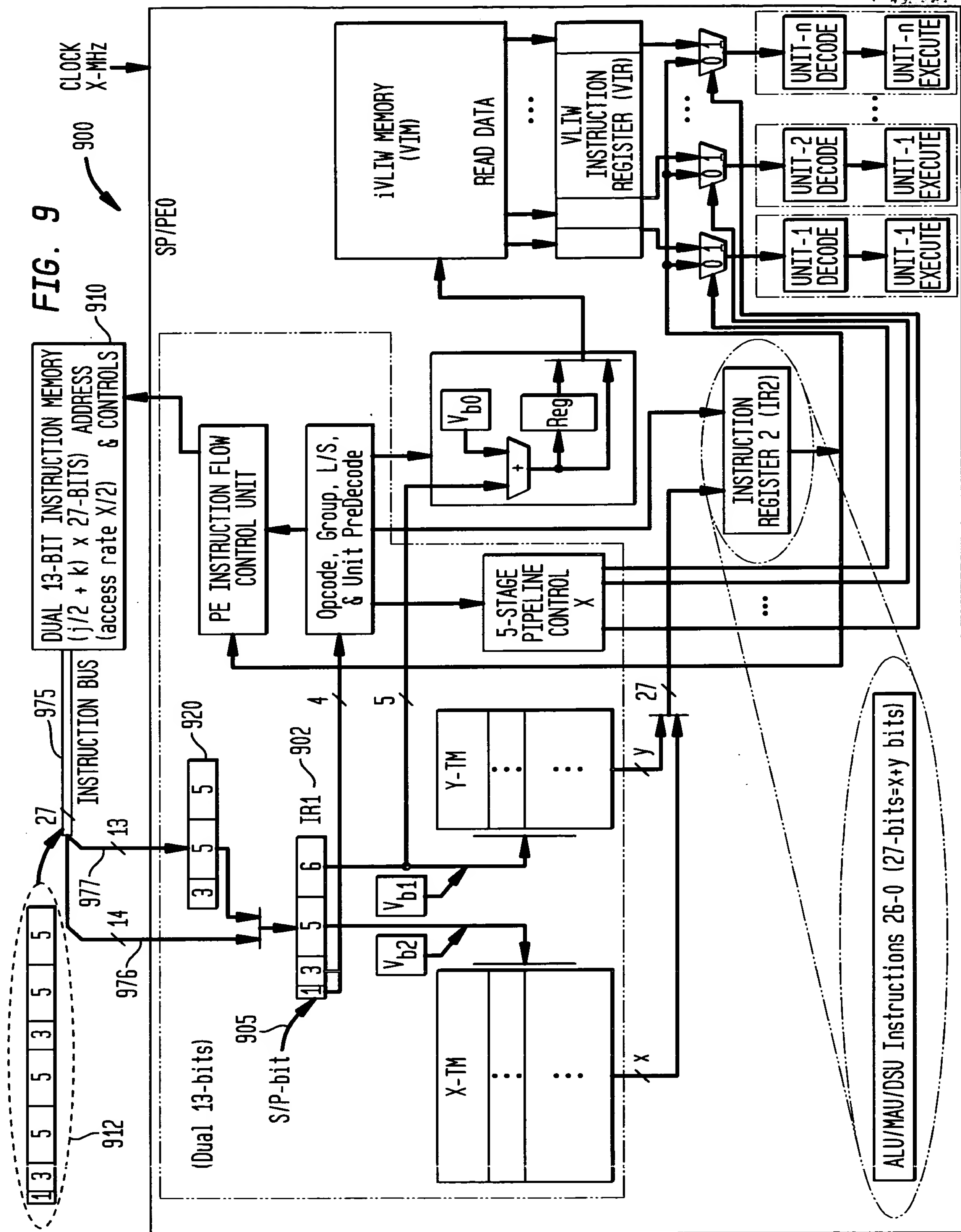


FIG. 10

CYCLE	FETCH	Xpand & Dispatch	Decode	Execute	Cond. Ret
i	SP Fetches a B-bit Instr(i)=ADD.S instruction & loads it into IR1	Previous Instruction Instr(i-1)	Previous Instruction Instr(i-2)	Previous Instruction Instr(i-3)	Previous Instruction Instr(i-4)
i+1	SP Fetches a B-bit Instr(i+1)=XV.S instruction & loads it into IR1	S/P-bit indicates an SP only operation. Local TM fetches occur and a native form of the Instr(i)=ADD.S instruction is loaded into IR2. The S/P-bit and 3-bit opcode are decoded in the S/P.	Previous Instruction Instr(i-1)	Previous Instruction Instr(i-2)	Previous Instruction Instr(i-3)
i+2	SP Fetches a B-bit Instr(i+2)=COPY.S instruction & loads it into IR1	S/P-bit opcode indicate an SP XV operation. Local TM fetches occur and a native form of the Instr(i+1)=XV.S instruction is loaded into IR2. The S/P-bit, and 3-bit opcode are decoded in the S/P. The VIM address is calculated and the iVLW is fetched from the XV VIM	The ALU decodes Instr(i)=ADD.S instruction	Previous Instruction Instr(i-1)	Previous Instruction Instr(i-2)
i+3	SP Fetches a B-bit Instr(i+3)=ADD.S instruction & loads it into IR1	S/P-bit indicates an SP only operation. Local TM fetches occur and a native form of the Instr(i+2)=COPY.S instruction is loaded into IR2	Instr(i+1)=XV.S causes up to 5 instructions in iVLW decode	The ALU executes Instr(i)=ADD.S instruction	Previous Instruction Instr(i-1)
i+4	SP Fetches a B-bit instruction: Instr(i+4)	S/P-bit indicates an SP only operation. Local TM fetches occur and a native form of the Instr(i+3)=ADD.S instruction is loaded into IR2	The DSU decodes the Instr(i+2)=COPY.S instruction	Instr(i+1)=XV.S causes up to 5 instructions in iVLW execute	Instr(i+1)=ADD.S side effects are set in ASFs and ACFs